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A HIGH EFFICIENT IMPROVED SOFT SWITCHED INTERLEAVED BOOST CONVERTER

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ABSTRACT

In this paper an improved ZVT interleaved boost PFC topology is introduced. The proposed ZVT interleaved boost converter is composed of two cell boost conversion units and an active auxiliary circuit. The proposed converter has two important advantages over the similar soft switching converters. The first one is that parallel to the main switches of the converter the auxiliary switch also operates under soft switching condition. Providing soft switching conditions for interleaved boost converters with more than one cells using only one auxiliary switch is another advantage of this topology. The prototype for the proposed converter was developed with an input of 110V ac power supply feeding a resistive output load of 600 watts. In addition, the proposed converter has the advantages of fewer structure complications, lower cost and ease of control.

Keywords— power factor correction, boost PFC converter, interleaved techniques, soft switching, zero-voltage-transition.

1. INTRODUCTION

Most electronic equipment is supplied by 50 Hz utility power, and more than 50% of this power is processed through some kind of power converter. Usually power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. Since these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment. These converters usually have a low power factor of 0.65. More stringent international requirements to limit the line input current harmonics, such as EN-61000-3-2 have been affected recently. Because the conventional simple diode rectifier followed by a bulk capacitor cannot meet the requirements, which have stimulated the research of power factor correction techniques.

The power factor is defined as the ratio of the average power to the apparent power at an AC terminal. When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the real power it consumes. This implies that the power source should be rated with higher VA ratings than the load needs. In addition, the current harmonics the converter produces deteriorate the power source quality, which eventually affect the other equipment. The simple solution to improve the power factor is to add a passive filter, which is usually composed of a capacitor and an inductor. However, this passive filter is bulky and inefficient since it operates at the line frequency. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. The PFC technique reduces current harmonics in utility systems produced by nonlinear loads.

Among the different alternatives, the boost converter operating in continuous conduction mode (CCM) has been widely adopted as a front-end PFC pre regulator [1, 2].The favorable features of boost converter are simple topology, high power density, fast transient response and continuous input current. Therefore, boost converters are usually used in different power electronics applications such as active

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PFC, photovoltaic power systems and fuel cells [3, 4]. Also interleaved operation (the parallel connection of switching converters) of two or more boost converters has been proposed to increase the output power and to reduce the output ripple. This technique consists of a phase shifting of the control signals of several cells in parallel operating at the same switching frequency [5]. As a result, the input and output current waveforms exhibit lower ripple amplitude [6].

High-switching-frequency operation is necessary to achieve small size of the converter. However, the switching loss will increase as the switching frequency is increased. To solve this problem, soft switching techniques are necessary. The zero-voltage-switched (ZVS) technique and zero-current-switched (ZCS) technique are two commonly used soft switching methods [7]. By adopting these techniques, either voltage or current is zero during switching transitions, which largely reduces the switching loss and also increases the reliability of the power supplies.

The choice of the soft-switching technique, i.e., ZCS or ZVS, it is taking into account the technology of the semiconductor device that will be used. For example, the Power MOSFETSs present a better performance when are commutated under ZVS, since they exhibit turn-on capacitive losses when operating in ZCS increasing the switching losses and EMI. On the other hand, the IGBTs present better results when are commutated under ZCS which can avoid their lath up and the turn-off losses caused by the tail current. Nevertheless, the ZCS techniques have some drawbacks such as, a significant voltage stress on the main diode, which increases the conduction losses, and the presence of the resonant inductor in series with the main switch, which increases the magnetic losses[8]. The technique of zero voltage switching is applicable to all switching topologies. ZVS technique basically consists of forcing to zero the active switch voltage, prior to its turn-on, by creating a resonance between an inductor and a capacitor. The inductor also limits the rate of variation of the diode current, so losses due to the reverse recovery are reduced as well [9, 10].

2. PROPOSED TOPOLOGY

In the proposed circuit diagram, the diode bridge rectifier is used to convert the ac line input voltage to the dc value. The circuit consists of two cell interleaved boost converters. With the help of this interleaving technique, inductor current of interleaved boost converter can be reduced. Thus result in reducing inductor size.

The main switches of the converter, M_1 and M_2 are gated with 180^0 phase shift with identical frequencies and duty ratios. The auxiliary circuit is added to two cell interleaved boost converter to reduce the switching losses. The auxiliary circuit consists of an auxiliary switch, an auxiliary inductor and a few other passive components. The auxiliary inductor L_r is required for the resonant process that discharges the drain source capacitance of the switch and for limiting the rate of change of the diode current at turn off. The auxiliary switch, Ma is gated with constant duty ratio just before the main switches. This initiates a resonant process, which creates zero voltage switching conditions for the main active switch. The time interval where the auxiliary circuit is active, is very short compared to the switching period.

In the previously implemented schemes, zero voltage switching condition for the main switch without increasing the voltage stress of the main and auxiliary switch is used [10,11]. The disadvantages of this converter is that the auxiliary switch operates under hard switching condition and this increases the EMI noise level and decreases the efficiency of the converter.

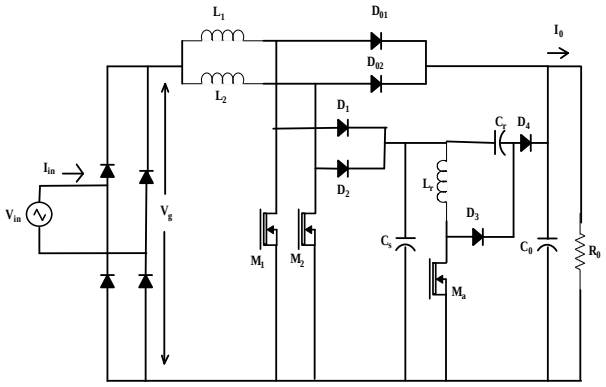

Figure. 1 Soft switched interleaved boost converter.

In the proposed interleaved ac-dc converter, the main switches uses zero voltage transition (ZVT) technique and auxiliary switches use the soft switching

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technique. The ZVT technique provides basically a perfect turn on process for the main switches of the converter [11]. Here there is no overlap between the voltage and current of the main switches and hence no switching losses take place at turn on process. So this converter has no additional voltage and current stresses and the efficiency is also improved.

The PFC control circuit includes the following control loops: Voltage Control Loop and Current Control Loop. The voltage control loop compares output voltage with reference and provides error to loop regulates the output voltage regardless of any variations in load current and the supply voltage. The output of the voltage control loop is a control signal, which determines the reference current for the current control loop. The function of the current compensator is to force the current to track the current reference that is given by the multiplier and which has the same shape as the input voltage. The feed forward loop is inserted to compensate the line voltage variation. The output of the current compensator decides the duty cycle 'D' required for switching the MOSFETs. The output from the current controller loop is compared with the saw tooth wave and produces the corresponding PWM signals. It is phase shifted and is given to two main switches. The auxiliary switches receive the gate from a logic circuit present in phase shifting controller.

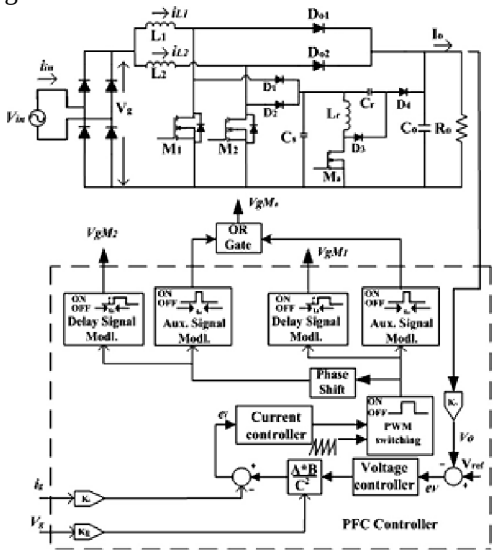

Figure. 2. Power circuit and control circuit of the proposed topology

3. DESIGN PROCEDURE

The design procedure for the proposed soft switched interleaved boost converter operating in continuous conduction mode (CCM) is presented in this section.

1. Operating requirements:

Pout (max):	600W
Vin range:	110-220VAC
Line frequency range:	50Hz
Output voltage:	400VDC

2. Switching frequency:

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20 KHz to 300 KHz proves to be an acceptable compromise [12]. This converter uses a switching frequency of 50 KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive.

Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubber for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency. For designing purpose here we consider the worst case, (Low input voltage and high input current).So we select, switching frequency, f_s=50 kHz

Input and output parameters:

The relationship between the duty cycle and the output/input ratio for interleaved boost converter is

$$Vo = \frac{}{} * V_g \quad (1)$$

Iin=5.59A given

$$Deff = 1 - \frac{}{} = 0.72024 \quad (2)$$

$$\text{Rectified voltage, } Vg = |Vm * \sin 2\pi f| \quad (3)$$

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$Vg = |110 * \sqrt{2} * \sin(2 * \pi * 50)| = 11.6021$ V

Output current, $Io = \mu(1 - Deff)Iin = 1.6$ A

Output power, Po = Vo * Io = 601.24W
(4)

Vo = Io * Ro (5)

From the above equation, Ro = — = 250 Ω

Selection of boost inductor:

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak current of the input sinusoid [13]. The maximum peak current occurs at the peak of the minimum line voltage and is given by

$$Ipk = \sqrt{2} * \frac{Pin}{Vin(min)}$$

Where Pin = Pout (max) (6)

Ipk = √2 * — = 7.7138 A

Inductor current ripple, $\Delta IL = 0.2 * Ipk = 1.54$ A

L = Vin * —— = 1452μH

L1 = L2 = L / 2 ≅ 700μH

Selection of Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time[14]. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical [15].

Hold-up time, Δt = 25msec

Assuming the efficiency of converter as 96.12 %,

$$Co = 2 * Pout * \frac{\Delta t}{\square * (Vo - Vo\ min)} \approx 470\mu F$$

Selection of snubber capacitor and resonant circuit:

Select Cs a small value so that Cs=1.1nF. Desired delay time (td) should be less than 10 percent of switching period. So = 0.86μsec.

Time delay, td ≥ * — + π * √(Lr * Cs) (7)

After calculation, ≅ 15μ

Also fundamental impedance, Z ≤ 60.So we select

Z= 40Ω and Z = √—

Cr ≈ 10nF

Output voltage ripple alculation:

= * * ——
* *

= 0.0165V

4. SIMULATION RESULTS

The computer simulation of proposed converter is done using Mat lab/Simulink and the results are presented. The simulation result of input voltage and input current is shown in figure 3(a) and figure 3(b) respectively. The simulation result of output voltage, output current, output of pulse generators are shown in figure 3(c), figure 3(d) and figure 3(e) respectively.

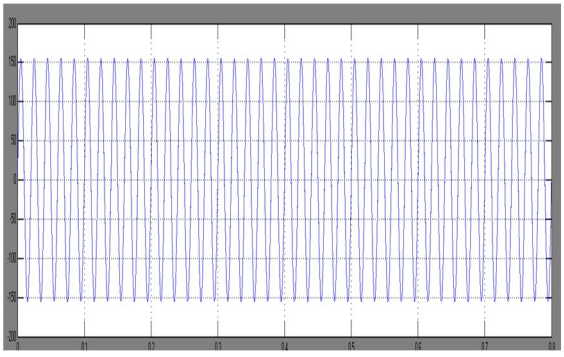

Figure 3(a) Simulation result of input voltage.

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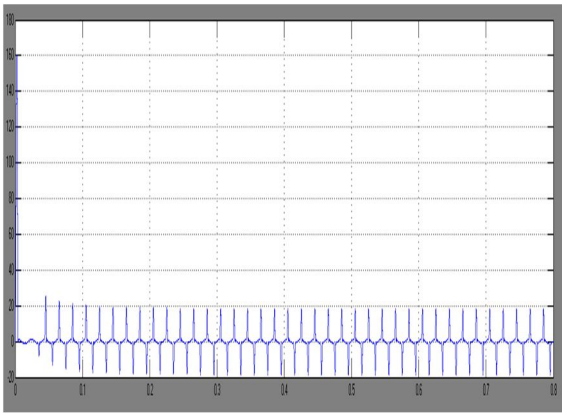

Figure 3(b) Simulation result of input current

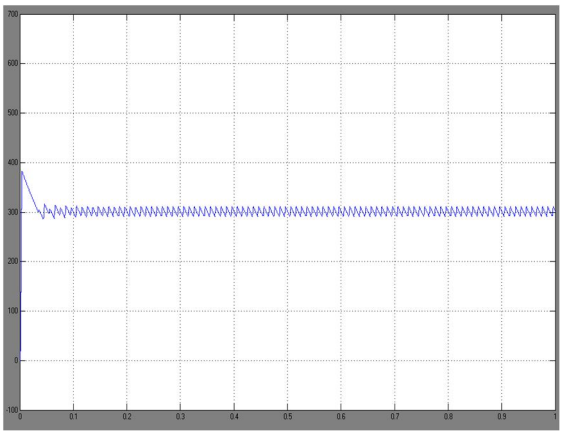

Figure. 3(c) Simulation result of output voltage

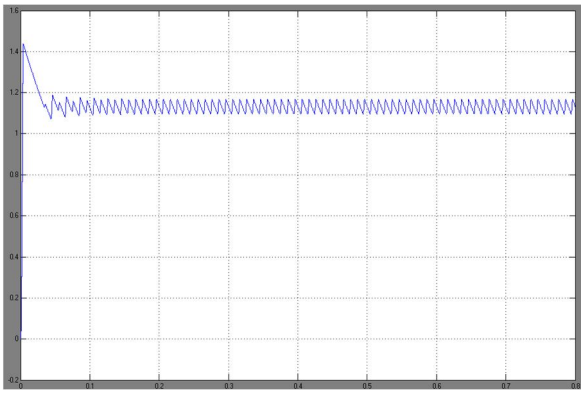

Figure 3(d) Simulation result of output current

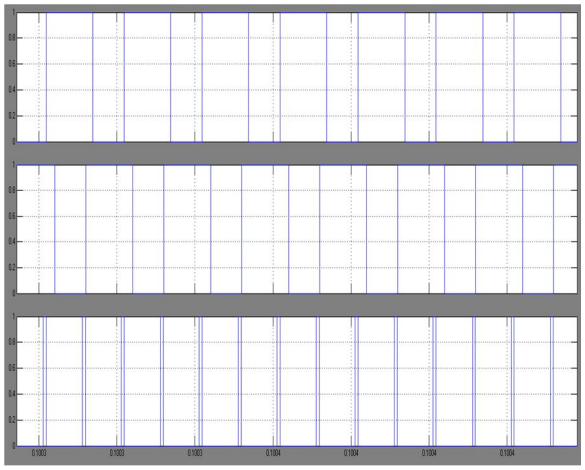

Figure. 3(e). Simulation result of pulse generators

Table 1. Comparison of performance of open loop and closed loop configurations

Types	Power factor	Efficiency (%)	THD (%)
Without PFC controller (open)	0.98	54	132
With PFC controller (closed)	0.999	77.5	34.26

5. CONCLUSION

In this paper an improved ZVT interleaved boost PFC topology is introduced. The computer simulation of the converter has been carried out using Matlab7.10R2010a/Simulink. From the results, it can be seen that the main switches are turned on with ZVT and turned off with ZVS. Also, the auxiliary switch and the other diodes in the auxiliary unit are turned on and off with ZVS.This soft switching of the auxiliary switches is the main advantage of the proposed topology. The soft switching of the output diodes also reduces switching losses. The simulation results show that the total switching losses of the hard switched interleaved topology is reduced by the use of the proposed auxiliary circuit. Using only one resonant

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inductor and minimum number of components in the auxiliary circuit does not result in a bulky converter. The prototype of the proposed topology has been designed and experimental study is under progress.

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